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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,290	02/28/2006	Adrianus Josephus Bink	NL031031	5446

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2109	

NOTIFICATION DATE	DELIVERY MODE
09/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/570,290	BINK ET AL.	
	Examiner	Art Unit	
	Mark A. Giardino	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 February 2006 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The drawings are objected to because there are no reference characters as required by 37 CFR 1.87(p). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37

CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

The disclosure is objected to because of the following informalities: misspellings or grammatical errors on Page 1 Line 13 ('purpose'), Page 2 Line 12 ('mention'), Page 4 Line 22 ('preformed'), and Page 5 Line 10 ('part').

Appropriate correction is required.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The term 'reduction mapping' is not well known in the art, nor is it explained clearly enough in the specification as it applies to the remapping means of Applicant's invention.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-5, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lefsky (US 5,019,971).

Regarding Claim 1, Lefsky teaches an integrated circuit, comprising:

-at least one processing unit (CPU 10)

-a cache memory having a plurality of memory modules for caching data (cache memory 16)

-remapping means for performing an unrestricted remapping within said plurality of modules (element replacement control unit 58, also see Column 3 Lines 16-19 and Column 8 Lines 63-65).

Regarding Claim 2, Lefsky teaches all limitations of Claim 1, wherein said cache memory is a set-associative cache (Column 2 Lines 56-59).

Regarding Claim 5, Lefsky teaches all limitations of Claim 1, further comprising:

a Tag RAM unit associated to said cache for identifying which data is cached in said cache memory (embedded within the cache memories 40, 42, and 44; see Figure 2A) and

wherein said remapping means is arranged in series with said Tag RAM unit (the Tag RAM unit and element replacement control unit 58 are clearly in series, see Figure 3).

Regarding Claim 7, Lefsky teaches the integrated circuit according to Claim 5, further comprising:

a look up table for marking faulty memory modules (implemented using the 'status field' registers in the cache memories, which contains a bit indicating whether the entry is operational, see Column 5 Lines 3-16).

Regarding Claim 8, Lefsky teaches a method of cache remapping in an integrated circuit having at least one processing unit (CPU 10); a main memory for storing data (main memory 12) and a cache memory having a plurality of memory modules for caching data (cache memory 16), comprising the step of:

performing an unrestricted remapping within said plurality of memory modules (element replacement control unit 58, also see Column 3 Lines 16-19 and Column 8 Lines 63-65).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over common knowledge in the art.

All limitations of Claim 1 have been discussed above. It appears, even though not mentioned specifically, that the remapping means taught by Lefsky employs reduction mapping. However, in the event Lefsky does not, nevertheless, because reduction mapping ~~is~~ was notoriously well known in the art, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to have used reduction mapping to remap the defective cache cells. As motivation, reduction mapping requires fewer wires and registers, thus reducing area and cost of the circuitry. So, by using reduction mapping, additional benefits are obtained.

Claims 5 is rejected under U.S.C. 103(a) as being unpatentable over Asher in view of Kramer (US 4,868,869).

Regarding Claim 5, all of the limitations of Claim 1 have been discussed above. However, Lefsky does not teach a Tag RAM in parallel with said remapping means. Kramer teaches several lookup tables and additional circuitry (which is what a Tag RAM unit and a remapping unit with Map RAM are) connected in parallel (see Figure 9 in Kramer). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to have placed the Tag RAM and remapping means of Lefsky in parallel as taught by Kramer. As motivation, connecting circuitry in parallel generally leads to a faster circuit. Thus, by putting the units in parallel, additional benefits are obtained.

Claims 1-3 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Asher (US 6,671,822).

Regarding Claim 1, Asher teaches an integrated circuit, comprising:

-at least one processing unit (see Column 3 Lines 55-57);

-a cache memory having a plurality of memory modules for caching data (cache 15)

-remapping means for performing an unrestricted remapping within said plurality of modules (access control logic 12 along with multiplexers 22, 24, 26, and 28, also see Column 3 Lines 64-67 and Column 6 Lines 21-22).

Regarding Claim 2, Asher teaches all limitations of claim 1, wherein said cache memory is a set associative cache (see Column 3 Lines 12-13).

Regarding Claim 3, Asher teaches all limitations of Claim 1, wherein said remapping means is adapted to perform the remapping means on the basis of a programmable permutation function (see bus 18 in Figure 2, which uses a multiplexer to permute way 0 to another given way; it is the multiplexer select bits that enable this permutation mapping to be programmed).

Regarding Claim 8, Asher teaches a method of cache remapping in an integrated circuit having at least one processing unit (see Column 3 Lines 55-57); a main memory for storing data (not explicitly stated but understood to be present, see description of the benefit of having a cache in addition to a main memory in Column 2 Lines 11-14) and a

cache memory having a plurality of memory modules for caching data (cache 15), comprising the step of:

performing an unrestricted remapping within said plurality of memory modules (performed by access control logic 12 along with multiplexers 22, 24, 26, and 28, also see Column 3 Lines 64-67 and Column 6 Lines 21-11).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brenza teaches a way of remapping faulty modules. Bhavsar teaches a cache that remaps faulty modules to spare modules. Emma teaches a way of remapping caches based on congruence classes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Giardino whose telephone number is (571) 270-3565. The examiner can normally be reached on M-R 7:30 - 5:00. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached at (571) 272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M.A. Giardino

9/11/2007

DAVID L. ROBERTSON
SUPERVISORY PATENT EXAMINER